

# A Configurable Networks-on-Chip Router Using Altera FPGA and NIOS2 Embedded Processor

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**Abstract**—In this paper, we introduce a communication IP for System-on-Chip (SoC) namely Configurable Network-on-Chip Router (CNoC-Router), which can perform various kinds of topology configuration for an on-chip network. With the flexible topology configuration and an adaptive routing scheme, CNoC-Router can enable a network with high performance using a relatively easy control. Synthesizable Register-Transfer-Level (RTL) coding was designed and verified with ModelSim. Furthermore, a prototype based on Altera FPGA with a NIOS2 embedded processor has been implemented to demonstrate its practice.

**Keywords**—Embedded Processor; Field Programmable Gate Array; Networks on Chip; Router; System on Chip

## 1. INTRODUCTION

Embedded devices usually run just one or a few applications. Therefore, general-purpose processors are not suitable for running those applications because they are either too slow or too power hungry. Low-power embedded processors combined with hardware accelerators are the preferred choice for most designers. Recent designs for the embedded market use multi-core microprocessor to reduce power consumption. Future embedded systems may use a large number of heterogeneous cores to deliver the best trade-off between performance and power consumption. For these reasons, this paper presents a Configurable Networks-on-Chip Router (CNoC-Router) implemented by Altera FPGA [1] (Field Programmable Gate Array) and cooperating with a NIOS2 [2] embedded processor to demonstrate its function correctness and application extension for the many-core paradigm.

## 2. BACKGROUND

From on-chip interconnection networks [3] to the Networks-on-Chips (NoC) paradigm [4], packet switching is an aggressive, long-term approach for nano-scale interconnection networks [5]. To exchange messages among cores, the CNoC-Router was designed to transmit and receive packets through the physical interconnection channels between routers in the network. In contrast to the computer network, CNoC-Router covers functions of not only the data-link layer, but also the network layer to offload the processing overheads (e.g., packet routing procedures and switching controls) in embedded processors. In following sections, we will introduce the proposed techniques and demonstrate the enhanced network performance. Finally, a conclusion will be drawn.

## 3. ARCHITECTURE

CNoC-Router is a 5 five port router as shown in Fig. 1. In which, Port 0 can be attached to a host entity (i.e., processor), Port1~Port4 are used to connect to neighbour routers.

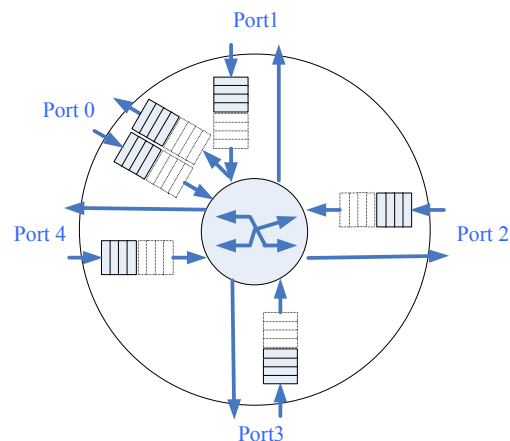


Fig. 1 A five-port router

### 3.1. Applicably Topology

By using CNoC-Router, various kinds of topologies can be configured, implementation examples are shown in Fig 2.

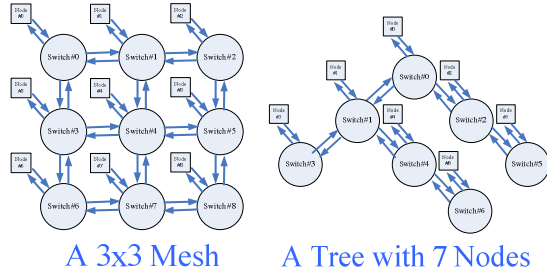


Fig. 2 Topology examples

### 3.2. Router Interface

Host/Neighbour-Router interfaces contain wrappers for each master and slave controller to transform Host/Neighbour-Router signals for the FIFO controls. Most kinds of processors can be attached to the CNoC-Router with little interface design modifications. In this paper, the Host interface is fitted to an Altera NIOS2 embedded processor.

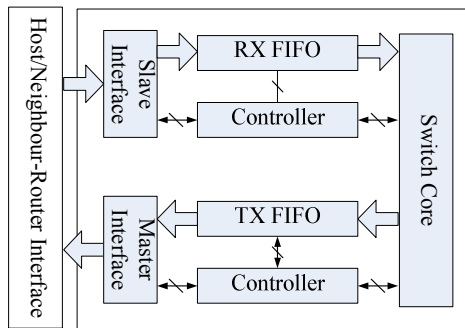


Fig. 3 Host or router interface of the router

### 3.3. Switching Core

The router switching core includes Arbiter, Routing Table, Control Registers, RX FIFOs, Interface Controllers, and Multiplexers as shown in Fig4.

## 4. SPECIFICATION

Encapsulation and routing for packets are two essential functionalities of the designed router. Next, the proposed specifications are introduced as follows.

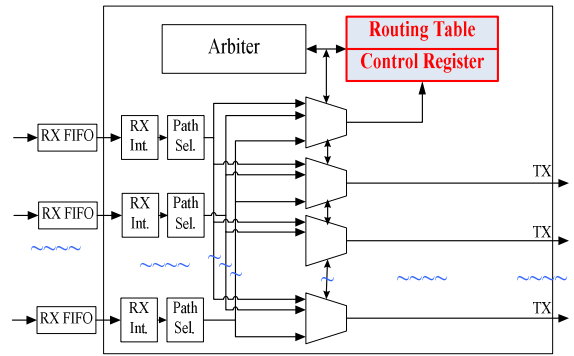


Fig. 4 Switching core

### 4.1. Packet Format

Table 1 illustrates the packet format (32 bits/word), which can support up to 65536 ( $2^{16}$ ) routers addressed in a network, and a packet data length from 0 to 65535 ( $0 \sim 2^{16}-1$ ) flits. Besides, the Destination Offset is to support Direct Memory Access (DMA) between routers. The CRC (Cyclic Redundancy Check) field is used for packet error detection. Moreover, the Control Code field can enable an intelligent network system. For example, bits in the Control Code can be used to distinguish packet types (uni-cast, multi-cast, or broadcast), to record the packet sequence number (for packet retransmissions), to support Quality of Service (QoS), and so on.

TABLE 1  
PACKET FORMAT

<b>31</b>	<b>16</b>	<b>15</b>	<b>00</b>
Destination Address		Control Code	
Source Address		Data Length	
Destination Offset		Extended Control Code	
Data (0 - 65535 flits)			
...			
CRC (1 flit)			

TABLE 2  
ROUTER REGISTER

Name	Address	Description
Router Add.	0x0000	Router Address
Channel Num.	0x0000	Channel Number
TABDA3~0	0x0001	Destination Add. 3~0
TABDA7~4	0x0002	Destination Add. 7~4
TABDAb~8	0x0003	Destination Add. b~8
THPRI4~1	0x0004	Threshold of Pri. 4~1
Reversed	0x0005	Reversed
	~	
	0xFFFFE	
Testing	0xFFFF	For Testing

## 4.2. Router Register

Table 2 is the implemented router register table (32 bits/word). The registers can be programmed directly by the local host (i.e., the attached processor) or via a packet come from another router.

## 4.3. Routing Scheme

Each router owns a routing table (cf. TABD<sub>x</sub> in TABLE 2), which keeps the priority of output ports to other routers (the table is predefined according to the network topology). In general, the router chooses the first priority except the expected port is congested. This policy gives a router the ability to choose another path to avoid the heavy traffic region. Besides, the threshold (cf. THPR<sub>Ix</sub> in TABLE 2) of congested levels to enable a re-route can be adjusted. As Fig. 5 shows, when a packet in Router #0 and would like to go to Router #3, it will choose the path via Router #1 instead of Router #2, because Router #1's FIFO have more free space than that free FIFO space in Router #2.

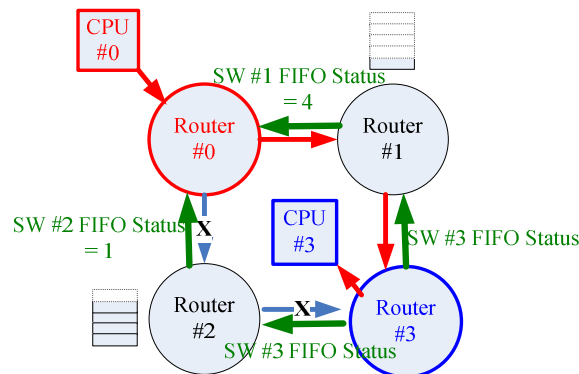


Fig. 5 Routing policy

## 5. PERFORMANCE ANALYSES

In this section, FIFO size, packet size, routing function, and FPGA performance of the implemented CNoC-Router are evaluated.

### 5.1. Analyses of FIFO and Packet Sizes

Referring to Fig. 6, we adopted a star topology with five routers as the analysis configuration and compared the performance results with a native switching method. The FIFO size can be programmed via a QUE\_LENTH parameter in the CNoC-Router RTL design, and the packet size can be adjusted in the Data\_Length field of the proposed packet header (cf. Table 1).

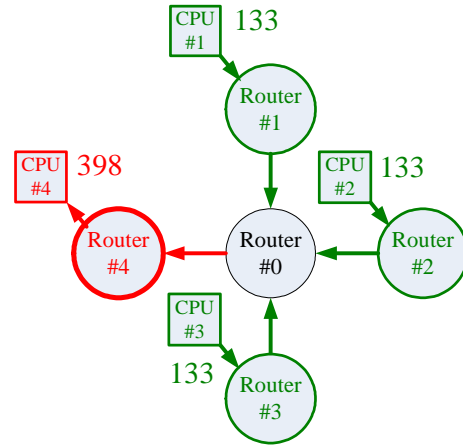


Fig. 6 Configuration of size effect analyses

The first diagram in Fig. 7 shows that a larger FIFO size has higher traffic variations tolerances compared with a small size FIFO. According to the second diagram in Fig. 2, transmissions with bigger size packets (16 words per packet) achieve superior transit throughput due to less arbitration transition overheads in routers.

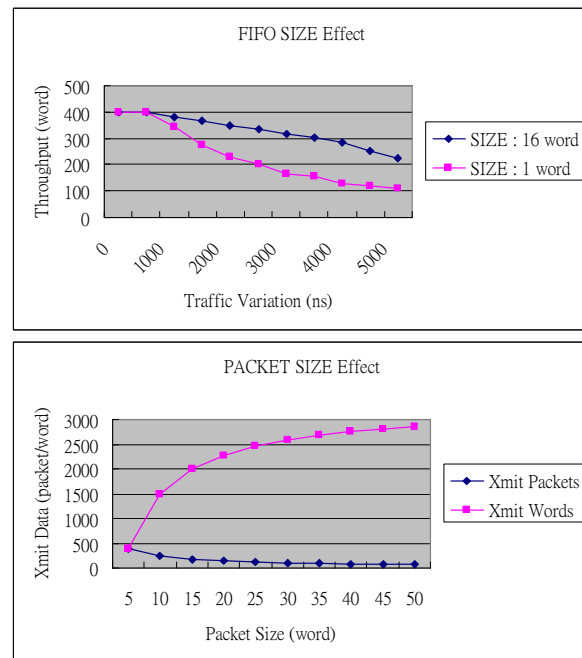


Fig. 7 Performance analyses of diverse FIFO sizes and packet sizes

### 5.2. Analyses of Adaptive Routing

In Fig. 8, CPU #0 at Router #0 issues packets to CPU #3 at Router #3. There are 3 paths to be selected. We list the paths from the shortest to the longest as follows: Path1 (#0 → #1 → #2 → #3), Path2 (#0 → #4 → #5 → #2 → #3), Path3 (#0 →

#4 → #6 → #7 → #2 → #3). As the number above the Router #3 shows, CPU #3 received 397 packets during 100 us simulation time, most of them are coming via the shortest path (Path1).

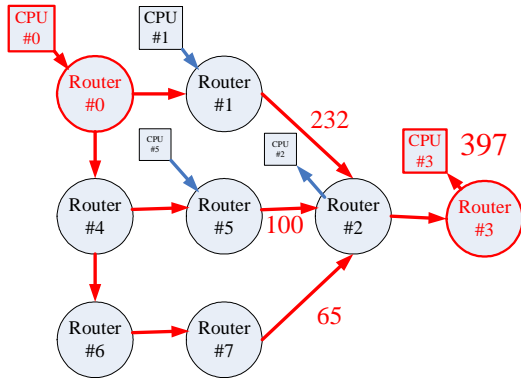


Fig. 8 Configuration of adaptive routing analyses

Next, we enforced local traffic jams on Path1 (Router #1 to Router #2) and Path2 (Router #5 to Router #2) as shown in Fig. 9. We found that packets can be rerouted to another passable path (i.e., Path3) to avoid the hot traffic spots. The total packets received by CPU #3 are decreased slightly in the identical simulation time of 100 us.

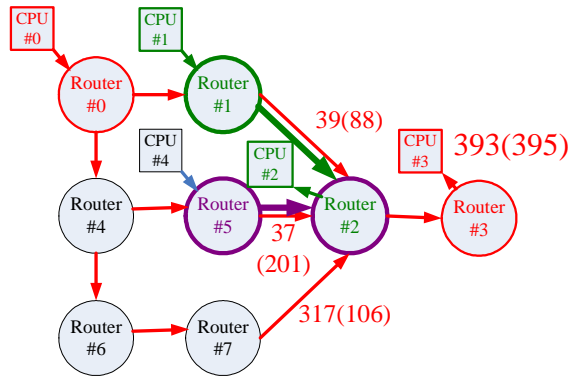


Fig. 9: Routing analyses with local traffic jams

### 5.3. Analyses of FPGA Performance

The CNoC-Router was designed in Register-Transfer-Level (RTL), verified with ModelSim [6], and implemented by Altera FPGA [1]. We list the FPGA performance indexes in Table 3.

TABLE 3  
FPGA PERFORMANCE

Tool	Quartus II Version 7.2
Device	Stratix II, EP2S90F1020C5
Utilization	14 %
Frequency	76.38 MHz

The maximum operation frequency is 76.38 MHz, which is large than the FPGA board clock rate of 50 MHz. The delay of the design critical path can be greatly reduced in an Application Specific Integrated Circuit (ASIC) design.

## 4. CONCLUSIONS

In this paper, a Configurable Network-on-Chip Router (CNoC-Router) was proposed to support an on-chip, packet-switching based network infrastructure for the coming many-core system-on-chip designs. CNoC-Router supported with packet routing and switching are functions corresponding to the network and data-link layers. Evaluations on comprehensive traffic patterns showed that CNoC-Router can enhance network performance by well setting the router's configurable control register set. Besides, the designed packet format reserved many fields for further extensions. We believe that such a flexible architecture of CNoC-Router will support advanced applications and satisfy diverse communication requirements in the next-generation deep-submicron chip designs.

## ACKNOWLEDGMENT

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