

# 1.5V Square-Root Domain Band-Pass Filter With Stacking Technique

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**Abstract**— A low voltage square root domain filter based on the MOSFET square law is proposed. Through the verification of HSPICE simulation, the extendibility and the reliability of the design procedure are proven.

A design technique for current-mode square-root domain band-pass filter simulation in a 0.18  $\mu\text{m}$  CMOS process. The basic building block consists of current-mode current mirrors, square-root circuit and capacitors. the prototype of the band-pass provides tunable center frequency of 2.19-3.49MHz with bias-current-tunable, -33.9dB total harmonic distortion (THD), and approximately 1.77 mW power dissipation with a 1.5 V supply voltage. Advantages of the proposed filter include high frequency operation, electrical tuneability, low supply voltage operation, and low power consumption.

**Keywords**— stack technique, square-root domain, band-pass filter, current-mode circuit

## 1. INTRODUCTION

Recently, due to the characteristics of high-frequency operation and tuneability, many researchers have devoted themselves in developing log-domain and square-root domain filters. Log-domain filter originally proposed by Adams [1] is a nonlinear (exponential) mapping on the state variables of a statespace (SS) description of a linear transfer function. Frey [2, 3] utilized the exponential transformation of the state space description of a linear transfer function, in terms of bipolar circuits, to implement log-domain filters and in turn, was embedded in as forming part of a broader branch of structures by Tsvividis [4]. Toumazou [5, 6] proposed a systematic synthesis method to implement log-domain filters based on “Bernoulli cell”. Germanovix [7] proposed a log-domain

filter in terms of MOSFET circuits operated in weak inversion, but its operation is limited only to kilo hertz range. In order to improve the issue of Psychalinos [8], Yu [9] and Lopez-Martin [10,11] also adopted MOSFETs operated in saturation region to implement the square-root domain filters.

In this paper, a square-root domain filter scheme based on the MOSFET square law to implement the band-pass and is proposed. The aims are to establish an adjustable Q architecture and to increase the operation frequency. The presented circuits have the following merits: high frequency operation, tuneability, low supply voltage, and low total harmonic distortion. Moreover, this approach provides an alternative for realizing a low voltage continuous-time filter designed by standard digital CMOS technology and is suitable in system-on-a-chip (SOC) application.

## 2. PRINCIPLE AND ARCHITECTURE

The transfer function of a second-order band-pass filter can be expressed as

$$H(s) = \frac{(\omega_0)s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} \quad (1)$$

By using the standard technique for creating companion-form dynamical equations, Eq. (1) is realized with the system described by the following equations.

$$\begin{cases} \dot{x}_1 = -\omega_0 x_2 \\ \dot{x}_2 = \omega_0 x_1 - \left(\frac{\omega_0}{Q}\right)x_2 + \left(\frac{\omega_0}{Q}\right)u \\ y = x_2 \end{cases} \quad (2)$$

where  $x_1$ ,  $x_2$ ,  $y$ , and  $u$  are state variables, output

and input signals, respectively. If the node voltages  $V_1$  and  $V_2$  are assumed to be the state variables,  $x_1$  and  $x_2$ , and a voltage signal  $U$  denotes the input  $u$ , the Eq.(2) can be rewritten as

$$\begin{cases} C\dot{V}_1 = -C\omega_0 V_2 \\ C\dot{V}_2 = C\omega_0 V_1 - \left(\frac{C\omega_0}{Q}\right)V_2 + \left(\frac{C\omega_0}{Q}\right)U \\ y = V_2 \end{cases} \quad (3)$$

where  $C$  is a multiply factor.  $C\dot{V}_1$  and  $C\dot{V}_2$  in Eq.(3) can be regarded as the time-dependent current through the two capacitors  $C$  connected from  $V_1$  to ground and from  $V_2$  to ground, respectively.

The drain current of a MOSFET transistor operated in saturation can be expressed as

$$I_D = \frac{\mu_0 C_{ox} W}{2L} (V_{GS} - V_{th})^2 = \beta (V_{GS} - V_{th})^2 \quad (4)$$

where  $\beta$ ,  $V_{GS}$  and  $V_{th}$  are the device trans-conductance parameter, the gate-to-source voltage and the threshold voltage, respectively. Thus, the state-space equation becomes

$$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} - I_T \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \frac{\sqrt{I_0 I_2}}{Q} + \frac{\sqrt{I_0 I_U}}{Q} + I_T \\ y = V_2 \end{cases} \quad (5)$$

According to Eq. (4), and supposing  $Q=1$ , the state equations in Eq. (3) can be written as

$$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} - I_T \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \sqrt{I_0 I_2} + \sqrt{I_0 I_U} + I_T \\ y = V_2 \end{cases} \quad (6)$$

where

$$\begin{aligned} I_1 &= \beta (V_1 - V_T)^2 \\ I_2 &= \beta (V_2 - V_T)^2 \\ I_U &= \beta (U - V_T)^2 \end{aligned} \quad (7)$$

and

$$\omega_0 = \frac{\sqrt{\beta I_0}}{C} \quad (8)$$

$$I_0 = \frac{C^2 \omega_0^2}{\beta} \quad (9)$$

Note that  $\omega_0$  is inversely proportional to the capacitance  $C$  and is proportional to the square root of  $I_0$ ; hence the cutoff frequency  $\omega_0$  is dominated by the capacitance  $C$  and  $I_0$  is used to tune the cutoff frequency.

### 3. CIRCUIT IMPLEMENTATION

Fig. 1 shows a circuit diagram of the proposed band-pass filter. The band-pass is realized by using current mirrors, three current-mode square-root circuit blocks and two capacitors.  $V_2$  is the desired output voltage and  $U$  is a DC biased input voltage. The MOSFET current-mode square-root circuit is used to obtain the square-root of two currents. The DC bias current  $I_0$  is used for center frequency adjustment of this band-pass filter, whereas the current  $I_U$ ,  $I_1$  and  $I_2$  in the band-pass filter are related to the corresponding input voltages  $U$ ,  $V_1$  and  $V_2$ .

According to the MOSFET square law, the square-root of two current can be implemented by the current-mode square-root circuit as shown in Fig.2. The core circuit is composed of transistors M5, M6, M7 and M8. Assume that the aspect ratios of the transistors M7 and M8 are twice as many as M5 and M6, (i.e.  $\beta_5 = \beta_6 \equiv \beta$  and  $\beta_7 = \beta_8 \equiv 2\beta$ ) and the aspect ratios of transistors M12 and M13 are half as many as those of other transistors.

Hence from Fig. 2, we get

$$V_{GS5} + V_{GS6} = V_{GS7} + V_{GS8} \quad (10)$$

$$I_{SD7} = I_{SD8} \quad (11)$$

Based on Eq. (4), the source to gate voltages of transistors M5 and M6 can be expressed as

$$V_{SG5} = \sqrt{\frac{I_y}{\beta}} + V_T \quad (12)$$

$$V_{SG6} = \sqrt{\frac{I_x}{\beta}} + V_T$$

Alike, the drain currents of transistors M7 and M8 are equal to

$$I_{SD7} = I_{SD8} = 2\beta \left( \frac{V_{SG5} + V_{SG6}}{2} - V_T \right)^2 \quad (13)$$

Therefore,

$$I_{SD8} = I_{SD9} \quad (14)$$

$$I_{SD9} = 0.5I_x + 0.5I_y + \sqrt{I_x I_y} \quad (15)$$

Writing the KCL equation at the output node of this circuit, we can obtain

$$I_{out} = I_{SD9} - (0.5I_x + 0.5I_y) \quad (16)$$

which conforms the function of the current-mode square-root circuit operation.

### 4. SIMULATION RESULTS

Fig. 3 illustrates the simulated result of the current-mode square-root circuit while  $V_{DD} = 1.5V$ ,  $I_x$  and  $I_y$  are a triangle wave current with values between  $10 \mu A$  and  $50 \mu A$  and a  $50 \mu A$  DC current, respectively.

The circuit diagram of second-order band-pass filter is shown in Fig. 1. the simulated frequency responses of the band-pass filter with  $V_{DD} = 1.5 V$ ,  $C = 5 \text{ pf}$ ,  $Q = 1$ , while  $I_0$  is changed from  $30$  to  $50 \mu A$ , and simultaneously shows tuning of the center frequency  $f_0$  from  $3.69$  to  $5.49 \text{ MHz}$  of the band-pass filter, shown in Fig. 4.

The total harmonic distortion (THD) with a  $4\text{MHz}$   $100\text{mV}$  peak-to-peak sinusoid is  $1.67\%$ . The specifications of second-order low-pass filter are shown in Table 1.

**TABLE 1.**  
**Specifications of the second-order band-pass filter**

Parameters	Simulation conditions
Filter order	2
Technology	TSMC $0.18\mu\text{m}$
Supply voltage	$1.5V$
Load capacitance	$5 \text{ pf}$
$I_0$	$30\text{ua}, 40\text{ua}, 50\text{ua}$
Parameters	Simulation results
$f_{3db1}, f_0, f_{3db2} (I_0=30\text{ua})$	$2.19 \text{ MHz } 3.69 \text{ MHz } 6.16 \text{ MHz}$
$f_{3db1}, f_0, f_{3db2} (I_0=40\text{ua})$	$3.00 \text{ MHz } 4.74 \text{ MHz } 7.38 \text{ MHz}$
$f_{3db1}, f_0, f_{3db2} (I_0=50\text{ua})$	$3.49 \text{ MHz } 5.49 \text{ MHz } 8.37 \text{ MHz}$
power dissipation	$1.54\text{mW}, 1.63\text{mW}, 1.77\text{mW}$
THD ( $V_{pp}=0.1V$ )	$1.71\%, 1.67\%, 1.95\%$
$f_{3db}$ tuning range	$2.19 \text{ MHz} \sim 3.49 \text{ MHz}$

### 5. CONCLUSION

In this paper, based on the MOSFET square law, on square-root domain band-pass filters is proposed. Band-pass filter operating at  $1.5V$  power supply voltage has been fabricated in  $0.18 \mu\text{m}$  CMOS technology; demonstrating the center frequency  $f_0$  is not only attainable at megahertz frequencies but also tunable electronically.

The proposed circuit, thus, has the advantages of operating at high frequency, at low supply voltage operation with low power consumption. Furthermore, the proposed filter implemented via standard digital CMOS technology offers a suitable solution for system-on-a-chip (SOC) application.

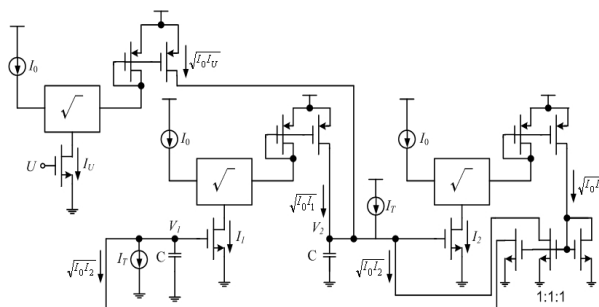
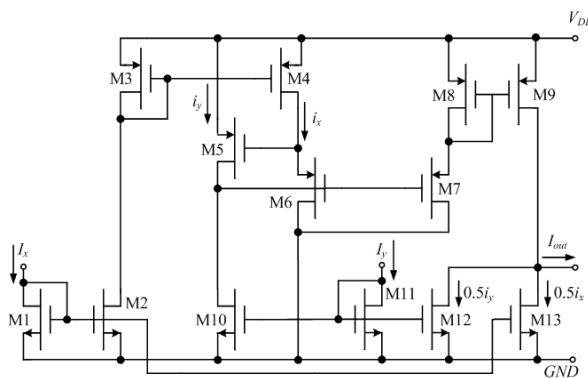
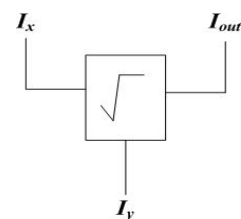


Fig. 1 Circuit diagram of the second-order band-pass filter



(a)



(b)

Fig. 2 Current-mode square-root circuit (a) circuit diagram, (b) equivalent block diagram

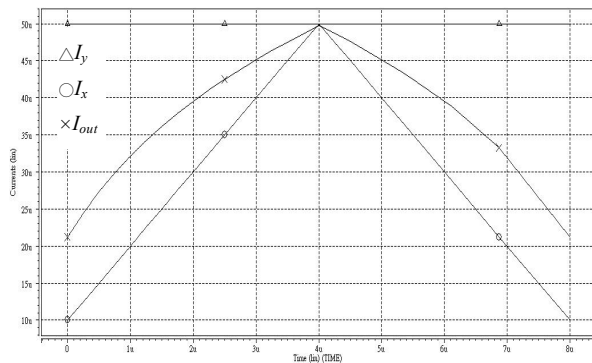


Fig. 3 Simulated result of the square-root circuit

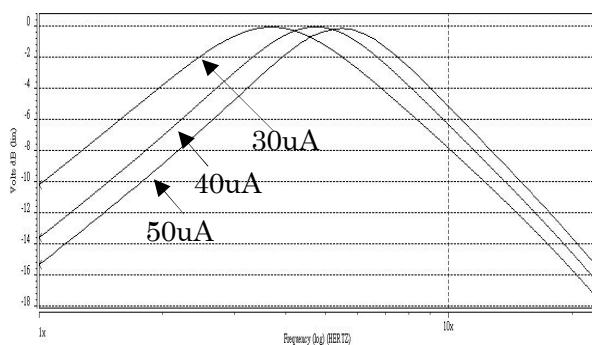


Fig. 4 Frequency response of the second-order band-pass filter

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