

Low Power Counter Design Using Wired Logic Circuit Technique

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Abstract—A novel extended true-single-phase-clock (E-TSPC) based divide-by-3 counter for low voltage and low power applications is presented. The basic idea is eliminating the extra logic gate between flip-flops to shorten the critical path, which facilitates a higher working frequency. Simulation results show that, when compared with conventional designs, as much as 23.1% saving in power-delay-product can be achieved by the proposed design. A divide-by-12 counter consisting of the proposed divide-by-3 counter design and two stages of asynchronous T-FF is developed and implemented in TSMC 0.18 μ m CMOS technology. The measured results show the design is capable of working at 500MHz when the supply voltage is only 0.6V.

Keywords—E-TSPC, low voltage, low power

1. INTRODUCTION

A high speed divide-by-N counter is a fundamental module for frequency synthesizers. It operates at a higher frequency and thus draws significant power consumption [1]. A divide-by-N counter consists of flip-flops (FF) and extra logic determining the terminal count. For the FF design, the extend true-single-phase-clock (E-TSPC) based FF has been considered a popular choice for high speed applications [2-6]. Compared to conventional TSPC designs, the E-TSPC design eliminates the transistor stacking structure to free all the transistors from the body effect. The E-TSPC design is thus more sustainable in low voltage operations [7-10]. The schematic of a conventional E-TSPC based divide-by-3 counter is shown in Fig. 1. The states of Q1b and Q2b cycle from 11, 01 to 00 and then return to 11 again for a new cycle. In addition to two FFs, two logic gates i.e. an AND gate and an inverter gate are needed. Past optimization efforts focused mainly on simplifying the logic gate structure to reduce both the circuit complexity and the critical path delay. For example, the E-

TSPC design uses one extra pMOS transistor to form an integrated function of FF and AND logic [3-4]. This measure, however, leads to an increase in both static and short circuit powers due to the ratioed circuit structure in FF designs [8-10]. In this paper, a novel circuit design technique to tackle the speed and power issues simultaneously is presented. Besides the two E-TSPC FFs, only one additional transistor is needed in the proposed design. The AND function is realized in a wired logic fashion without using any extra transistor. An always turn-on transistor is employed to avoid a possible reverse data between the FFs. The circuit complexity is greatly reduced, which results in a very compact layout and is beneficial to both operation speed and power consumption factors. The rest of the paper is organized as follows: In Section II, the proposed circuit technique and our design are described. In section III, post layout simulation results of the proposed design and prior art are presented. Various performance indexes are adopted to compare the merits of both designs and the measured results indicate undoubted advantages of the proposed design.

2. PROPOSED CIRCUIT DESIGN

The MOS schematic of the proposed E-TSPC based divide-by-3 counter is given in Fig. 2. The pMOS transistor P_{WIR} alone implements the required control logic. Refer to the MOS schematic shown in Fig. 1, an extra pull-up pMOS is added to the 1st stage inverter of FF2 to form a NAND logic. An inverter is needed to convert the polarity of signal Q1b. This calls for a total of three transistors to realize the control logic. In our design, signal Q1b is tied, through an always turn-on pMOS transistor, with the output node of the 1st stage inverter of FF2. Either Q2b equal to "0" or Q1b equal to "1" pulls the output node of the inverter high, which implements the logic $\overline{Q1-Q2b}$. The inverter needed to complement the Q1b signal is no longer needed.

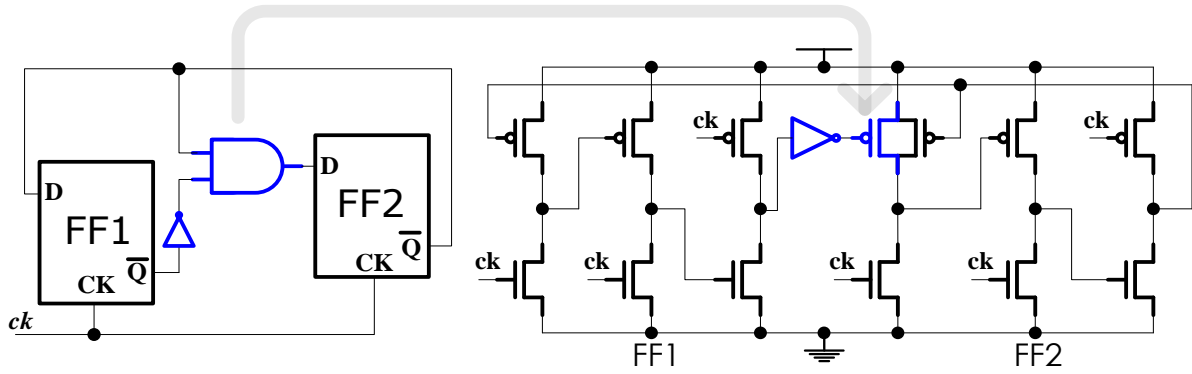


Fig. 1 Conventional E-TSPC based divide-by-3 counter design.

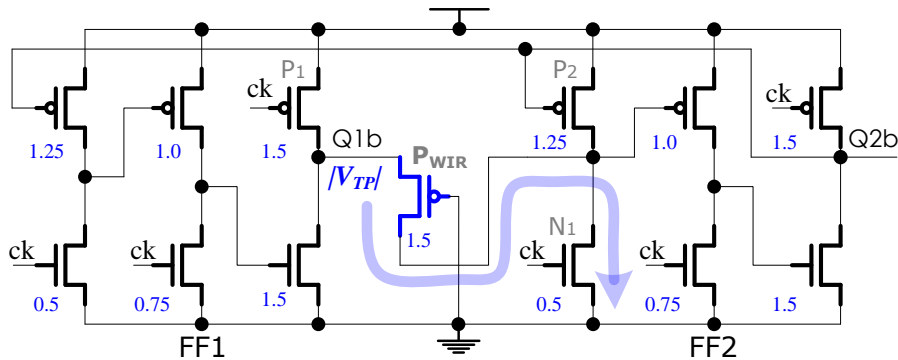


Fig. 2 MOS Schematic of the proposed E-TSPC based divide-by-3 counter design.

The always turn-on pMOS transistor P_{WIR} , though seems redundant in logic operation, serves to mitigate the erroneous discharge on node $Q1b$ by transistor $N1$. When $Q1b$ and $Q2b$ are both equal to “1”, transistors $P1$ and $P2$ are off, and node $Q1b$ is supposed to keep the state of $FF1$ on the parasitic capacitor. Without transistor P_{WIR} , a signal “0” flows backward to destroy the value of $Q1b$ when transistor $N1$ is turned by the clock signal. An always turn-on pMOS transistor, which can successfully pass a signal “1” forward, deters an intact “0” from flowing backward to node $Q1b$. As a result, node $Q1b$ is discharged from V_{DD} to $|V_{TP}|$ only. For low V_{DD} operations, the threshold voltage value is usually larger than one half of the V_{DD} . This value is even higher when taking the body effect into the account. The state “1” of $Q1b$ can thus be preserved and the proposed design functions properly, in particular for lower supply voltage operations.

3. SIMULATION RESULTS

Post-layout simulations in HSPICE were conducted to compare the performances between

the proposed design and the conventional design shown in Fig. 1. The target technology is TSMC 0.18 μ m 1P6M CMOS process. Transistor sizing is subject to power-delay-product performance (PDP) optimization and a typical-size inverter i.e. 1.5 μ /0.5 μ was used as the output load.

Fig. 3 shows the PDP of both designs versus V_{DD} . For low V_{DD} operations (less than 1.0 V), our design outperforms the conventional one in all voltage settings. For example, the PDP saving at V_{DD} equal to 0.9V is 15%. At the same voltage setting, the maximum frequencies of the proposed and the conventional designs are 2.48GHz and 2.35GHz, respectively.

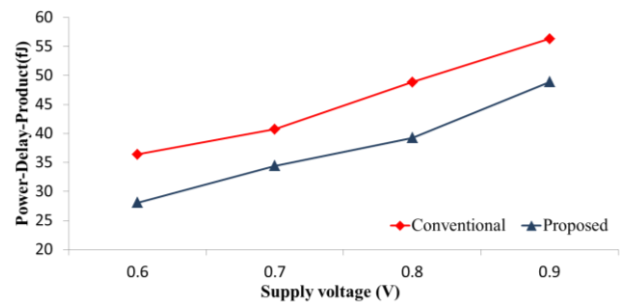


Fig. 3 PDP performances VS supply voltage.

TABLE.1 SIMULATION RESULTS AND FEATURES (@TT CORNER).

	Conventional	Proposed
Divide-by-3 Counters		
# of Transistor-Count / Area (μm^2)	15 / 86.08	13 / 70.87
Max. Frequency (MHz)	508	552
Average Power (μW)	18.38	15.44
Power-Delay-Product (fJ)	36.39	27.97

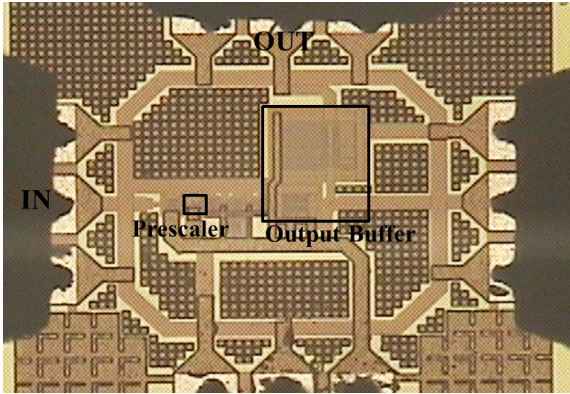


Fig.4 Die photo of the divide-by-12 counter.

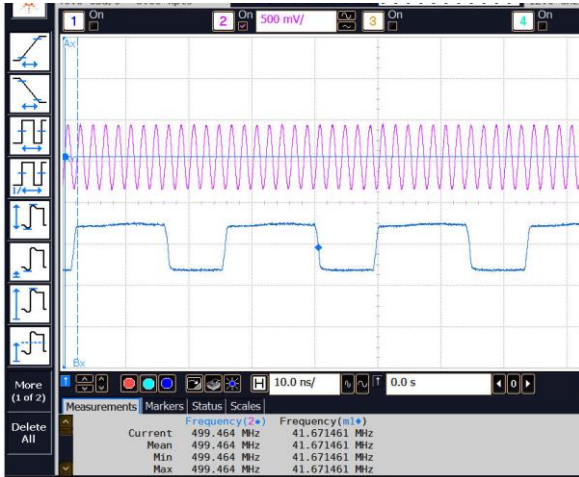


Fig. 5 Measured waveforms.

Table 1 summarizes the design features of both designs at V_{DD} equal to 0.6V. The proposed design excels in all design aspects. Its PDP number is 23.1% lower and the layout area is also 17.7% smaller. Numbers for other supply voltages also indicate a consistent performance edge of the proposed design. The proposed design is further extended to a divide-by-12 counter design by adding two stages of asynchronous FF (as divide-by-2 counter each). The extended design is fabricated using a TSMC 0.18 μm 1P6M CMOS process technology. The

die photo and the measured waveforms are shown in Fig. 4 and 5, respectively. The chip functions correctly at (0.6V/500MHz) and the measured power consumption is 16.75 μW . It is expected that the proposed design can be easily migrated to more advanced process technologies. This is because the threshold voltage does not scale proportionally to the V_{DD} scaling and thus provides even better isolation on the reverse signal flow across the P_{WIR} transistor.

4. CONCLUSION

A novel divide-by-3 counter design consisting of E-TSPC FFs plus an embedded wired NAND logic using only one pMOS transistor is presented. Simulation results show significant performance improvements against existing designs for low voltage operations. The design is further verified by real chip implementation.

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